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# Overview of Digital Design and Finite Element Analysis in Modern Power Electronic Packaging

Asger Bjørn Jørgensen, Stig Munk-Nielsen and Christian Uhrenfeldt

***Abstract*—Wide band gap semiconductors require packaging with reduced parasitic inductance and capacitance. To achieve this, new packaging solutions are proposed which increase integration. This causes difficulty in measurement of voltages, currents and device temperature, and therefore designers must rely more heavily on simulations to gain insight in the operation of the developed prototypes. Additionally, the use of digital design may reduce the number of physical prototype iterations and thereby reduces development time. Gaining fidelity of 3D multi-physics simulations, reduced order modelling and system simulation aids in the design of working prototypes and pushes performance of new power modules based on wide band gap semiconductor devices. This paper provides an overview and discusses the recent advances in the use of finite element analysis and simulation tools within the topic of power module packaging. The main aspects covered are extraction of electrical parasitics, simulation of transient thermal response and issues related to evaluation of electric fields. An example of a simulation software roadmap is presented which enables accurate electro-thermal simulation of new packaging structures that combine conventional power module technology with integrated printed circuit boards. The future challenges for utilizing the potential of digital design are discussed.**

***Index Terms*—Finite element methods, Design methodology, Semiconductor device packaging, Circuit simulation.**

## I. Introduction

DIGITAL design is receiving increasing attention from power module packaging and power electronic converter engineers. Digital design is the concept of using comprehensive simulations to accurately predict operation and rapidly improve the design, in contrast to building several physical prototypes to observe system performance. A reason for the increased interest in digital design, is attributed to research involved in the transition from using traditional silicon (Si) semiconductor devices to new wide bandgap (WBG) power semiconductors, based on materials such as silicon carbide (SiC) and gallium nitride (GaN). A key potential in the use of WBG semiconductor devices is reduced switching times and thereby lower losses, but this can only be achieved if the WBG devices are properly packaged and integrated in new compact packaging solutions [1], [2]. In recent years, several compact solutions have been proposed, such as: semiconductor dies embedded in printed circuit boards (PCB) [3]–[6], integrated direct bonded copper (DBC) modules [7]–[11] or hybrid structures combining PCB, integrated circuits (ICs), semiconductor and DBCs into a single switching cell [12]–[16]. The common goal for these packages is to obtain a low inductance power module capable of operating at high power and typically rated for voltages of 650-1200 V. In any case, the result is that many crucial parts are in closer proximity with one another and multi-physics coupling effects become more prominent.

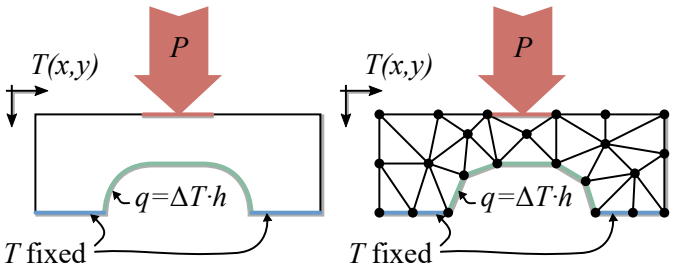


Fig. 1: An example of FEA by approximating a geometry with mixed boundary conditions into a number of simpler sub-domains which is easier to solve. $T$ is temperature, $P$ is power, $q$ is heat flux and $h$ is the heat transfer coefficient.

The mathematical expressions describing many of the physical phenomena such as thermal transport, electromagnetic fields and mechanical stress involve solving of partial differential equations. Such equations give the exact solution over a domain, but are also difficult to solve once the problem complexity increases, such as the representation of a real world problem including: advanced 3D geometries, mixed boundary conditions and varying material properties. Finite element analysis (FEA) is useful to solve and study such problems. The basic idea of FEA is to split the domain into smaller simple sub-domains called finite elements, as shown in Fig. 1, which are easier to solve for. The result is only solved at the nodal points, and thus piecewise continuous functions are used for interpolation, to approximate the value throughout the full domain. The size of the discretized elements, often referred to as the mesh, is flexible, such that it allows using more points in regions where steep gradients of variables are expected or higher accuracy is desired. Using multi-physics FEA simulation software to study problems such as electromagnetic fields or thermal behavior have become even more valuable for the designers of power module packaging or power PCBs for a number of reasons.

*Difficulty of measuring:* To utilize the fast switching speed of SiC and GaN, the inductance of commutation and gate loops are as low as only a few nH. This requires that

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A.B. Jørgensen, S. Munk-Nielsen and C. Uhrenfeldt are with the Department of Energy Technology, Aalborg University, Aalborg 9220, Denmark (e-mail: abj@et.aau.dk, smn@et.aau.dk, chu@et.aau.dk).

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the WBG devices are highly integrated in compact power modules, which causes difficulty in getting measurements of voltages and currents. Most current sensing techniques are intrusive, meaning that they need to be inserted in or around the current path, resulting in the addition of several nH to the commutation loop [17]–[19] and thereby might deteriorate the fast switching performance. The compactness of many new power modules and integrated packages causes difficulty in measuring internal states such as gate-source voltages, supply voltages or device temperatures. Similarly, identifying issues such as cross-coupling between internal PCB layers or ground plane bounce is difficult. In these cases the use of FEA might be the only solution to obtain such information about the design.

*Accuracy of measurements:* Even in the cases where measurement of voltages and currents of the WBG devices is possible, the accuracy of these measurements is of concern. Due to the compact layouts, resonance frequencies in power loops are increasing, and are excited due to the high $\mathrm{d}v/\mathrm{d}t$ and $\mathrm{d}i/\mathrm{d}t$ associated with steep transients during switching events. The frequency content exceed several hundreds of MHz which is approaching the limits for many >500 V probes which typically have a bandwidth in the range of 100-200 MHz for differential probes [20]–[22] and 400-500 MHz for passive probes [23]–[25]. Thus, as the limits of the equipment is approached, designers might start to lose trust in the measurements. Accurate simulations are a solution to regain trust, by adding another layer of validation to ensure that experimental measurements are correct.

*Computing power:* Using FEA to study such multi-physics problems on complex geometries have become more easily accessible. A major reason is that the number of available calculations per second is continuously increasing meaning reduction in simulation time. Combined with an increasing size of the memory, this allows even large and complex geometries to be studied. Engineers have often been required to simplify the problem and reduce the geometry to minor parts or two-dimensional (2D) cross-sectional studies, to reduce the simulation time and being able to store the problem in memory. Understanding the physics and having knowledge on a simplified model is important and cannot not be understated. However, it also limits the trust of how well the simplified model actually predicts the real-world behavior. The availability of desktop computers with quad/octo core CPUs and memory often in the range of 32 to 128 gigabytes means original geometries are solved for various physics with only minor simplifications.

This paper provides an overview of the simulation tools used to study the most common physics involved in the design of power module packaging. Key benefits for using power module packaging when compared to discrete packages include: reduction of electrical parasitics, improved thermal design and operation at high electric field strengths. Thus, electromagnetics parasitics extraction is covered in Section II. Calculation of thermal impedance and thermal coupling is described in Section III. Simulation of electric field density is discussed in Section IV, respectively. A main focus of the paper is reduced order modelling to allow combination of the obtained FEA results in an efficient multi-physics simulation environment. The recent advances within each topic are discussed in regards to power module packaging. In Section V the concept of digital design is discussed and a multi-physics simulation software roadmap is proposed, which allows for simulation of compact integrated power modules combining both PCB and DBC in a single switching cell. Future work is covered in Section VI. Finally the paper is concluded in Section VII.

## II. Electromagnetic finite element analysis

This section introduces the foundation of electromagnetism described by Maxwells coupled set of partial differential equations. This is followed by a brief discussion of various simulation software and how the equations are manipulated to allow solving for a given type of problem. In recent years ANSYS Q3D Extractor has been one of the most popular finite element method (FEM) software tools used for extracting electrical parasitics within power module packaging. In literature various approaches are used when working with ANSYS Q3D Extractor, and these approaches are categorized and discussed. Finally the use of extracted lumped electrical parameters in circuit simulators is presented.

Including of electrical parasitics has become more important as device sizes shrink, because the relative influence of the packaging becomes more prominent. In general, it is desired to reduce the electrical parasitics to enable an increase of $\mathrm{d}v/\mathrm{d}t$ and $\mathrm{d}i/\mathrm{d}t$ during switching. However, new problems arise as gate and power loops are reduced to similar low values in parasitic capacitance and inductance, meaning that the loop resonance frequencies start to merge. As described in literature for high $\mathrm{d}v/\mathrm{d}t$ operation of new WBG devices, they are prone to enter a self-sustained oscillating state if the size of parasitics are not controlled [26]–[29]. Thus packaging of the WBG devices is not simply a question of making the most compact layout, but also requires an in-depth understanding and analysis of the paths created by parasitic elements.

Fundamentally, all of the electromagnetic phenomena are described by Maxwells equations listed in a typical form as shown in (1)-(4).

$$\nabla \cdot \boldsymbol{D} = \rho \tag{1}$$

$$\nabla \cdot \boldsymbol{B} = 0 \tag{2}$$

$$\nabla \times \boldsymbol{E} = -\frac{\partial \boldsymbol{B}}{\partial t} \tag{3}$$

$$\nabla \times \boldsymbol{H} = \boldsymbol{J} + \frac{\partial \boldsymbol{D}}{\partial t} \tag{4}$$

A quick summary of Maxwells equations is given. Gauss' law (1) is relating the propagation of electric flux density, $\boldsymbol{D}$, from the distribution of electric charge density, $\rho$. It describes how electric field lines begin on positive electric charges and terminate at negative charges. Gauss' law for magnetism (2) states that the magnetic field, $\boldsymbol{B}$, does not begin or end. Faradays law of induction (3) defines how a time varying magnetic field induces an electric field $\boldsymbol{E}$. Finally Ampere's law with Maxwells addition (4) describes that a magnetic flux density $\boldsymbol{H}$ is generated in two ways, either by an electric

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current density, $\boldsymbol{J}$, or by a changing electric flux density, $\boldsymbol{D}$. The latter is often referred to as the *displacement current*.

For isotropic linear dielectrics and magnetic materials, the electric field $\boldsymbol{E}$ and magnetic field $\boldsymbol{H}$ are related to the electric flux density $\boldsymbol{D}$ and magnetic flux density $\boldsymbol{B}$ as

$$\boldsymbol{D} = \epsilon \boldsymbol{E} \tag{5}$$

$$\boldsymbol{B} = \mu \boldsymbol{H} \tag{6}$$

where $\epsilon$ is the permittivity and $\mu$ the permeability. The assumption of isotropic materials is often used as it simplifies analytical derivations. The assumption is also used within each node/cell of the finite element approximation, but material properties can be varied throughout the domain.

To extract the parasitic inductances and capacitances, it is required to solve (1)-(6). Depending on the frequency range that is of interest and the requirements to the accuracy, Maxwells equations are modified or only parts of the equations are studied without including the full coupling.

An approach is to use analytical equations, such as using simplified 2D geometries with assumptions of infinite long tracks with a uniform current distribution [30]. Several of such 2D segments are then connected to better represent the real structure. This can be a sufficient approximation for thin PCB traces at low frequencies, and the advantage is that parameters of thicknesses and lengths are explicitly available, thus are useful for early design optimizations of layouts [31]–[33]. Alternatively, for high accuracy of the real world problem, the original 3D geometry is imported to FEM software packages such as COMSOL Multiphysics [34] or ANSYS Maxwell [35]. This software solves a desired voltage/current distribution and provides transient full-wave solvers including non-linear material properties. The disadvantage is that such simulations can be time consuming, both in terms of time spent on setting up the model and its computational time.

Within power module packaging design, a popular approach is a compromise between accuracy and computational time, achieved using software packages such as FastFieldSolvers [36] (including the solvers FastHenry2 and FastCap2) or ANSYS Q3D Extractor [37]. These widely used software packages combine various finite element solvers to quickly extract electrical parasitics on complex 3D geometries. Linear material parameters are assumed and solutions are provided only at discrete frequencies. Systems are assumed quasi-static, meaning that the cross-coupled time-dependent terms of (1)-(6) are not included, i.e. magnetic fields are calculated without influence of changing electric fields but only depends on the defined current distribution. These software packages are specifically aiming at evaluating current distributions, electric fields and magnetic fields and converting them to quantities usually associated with electrical circuit diagrams, namely resistances, capacitances and inductances. These quantities are then recombined in the circuit simulator to produce a reduced order model of the system. ANSYS Q3D Extractor has lately been one of the most used software packages within power module design and is the main software package covered for this overview. The accuracy of the ANSYS Q3D Extractor solver has been studied in literature for case studies of power modules and TO-packages, and overall the conclusion is that the software provides a good approximation in the MHz-frequency range encountered in most power electronics applications [38]–[41]. The accuracy at higher frequencies can be improved by expanding the network into several RLC-segments, often referred to as a transmission line. In [38] good accuracy is achieved above 1 GHz by splitting a 2-inch-long trace of a PCB into 16 segments in ANSYS Q3D Extractor. The following section gives an overview of how the ANSYS Q3D Extractor is typically utilized in the literature, and highlights the advantages and disadvantages of each method.

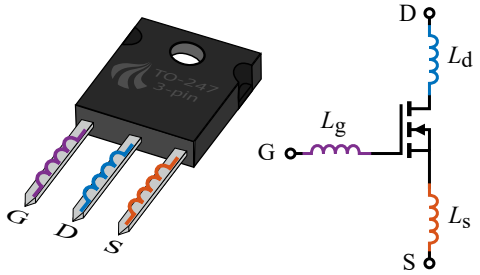


Fig. 2: Simulation method A calculating single piece-wise self-inductance values excluding coupling.

### A. Electrical parasitics evaluation in ANSYS Q3D Extractor

A literature review of research utilizing ANSYS Q3D Extractor indicates that the software package is used differently depending on the problem to be solved. In this section the methods have been classified into three different types.

*Method A:* A common way of representing the parasitic inductances of a circuit, is to evaluate the self-inductance of each trace/lead individually [16], [42]–[47]. In a circuit simulator these self-inductances are typically placed around the semiconductor die, similarly to what is shown in Fig. 2. In this overview, the approach is named as Method A. The advantage of this method is that setting up the simulation is simple and solving of the problem is fast, because it is distributed into single decoupled problems. The resulting inductance is easily read and placed as a lumped inductance in any circuit simulator. The disadvantage when using this approach is that it does not take into account the mutual coupling between the self-inductances. For many electrical layouts, they have been specifically designed in such a way that the magnetic fields are cancelled by clever design of the outgoing and returning current paths in the circuit. If the mutual inductive couplings are not included in the simulation circuit, it results in a wrong prediction of the effective inductance when current flows i.e. in a common drain and source path. Results of method A are easy to visualize as a schematic solely composed of lumped elements. It is useful in cases where modelling the magnetic field cancelling effects is not critical. For example in power modules with a single copper layer for the layout and largely spaced traces, and especially if the power module is operated at low $\mathrm{d}i/\mathrm{d}t$ where the contribution from the inductances are less dominant, such as in medium voltage power modules with tracks widely separated [31], [48].

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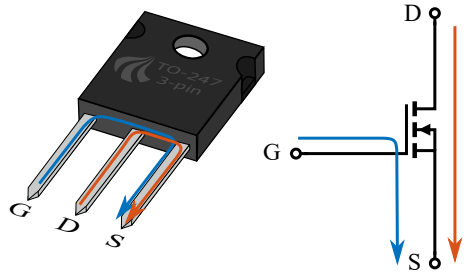


Fig. 3: Simulation method B calculates current loops.

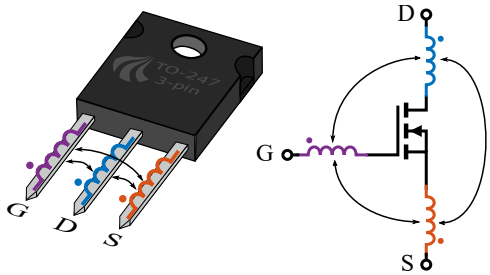


Fig. 4: Simulation method C calculates self-inductances and mutual inductance couplings.

*Method B:* To include the magnetic field cancelling effects of the designed layout, a method for calculating the effective inductance is by using the entire loop of interest in a single cycle [9], [32], [33], [42]–[44], [49], as shown in Fig. 3. For this overview the approach is defined as method B. The simulation cycle takes into account the magnetic coupling in the calculation of the inductance of the loop itself. In practice inside the simulation software, these loops are often created by shorting the terminals of the semiconductor die and assigning input/output of the loop on the pin ends. The disadvantage of this method is that the inductance is calculated for an entire path. This causes difficulty in implementing the calculated result in a circuit simulator, because it is no longer split into lumped elements that are easily placed around the semiconductor die model. The method is advantageous in optimization problems, where specific loops that are to be optimized are quantified by a single value read from the software. Typical applications are in the minimization of inductance in a commutation loop of a switching cell or gate-source loop. In these cases, method B makes it easy to visualize and provides more accurate results of the effective inductance when compared to method A.

*Method C:* This method uses the self-inductances similar to method A, but with the addition of coupling between each of the self-inductances [16], [46], [47], [49]–[53], as shown in Fig. 4. This method is defined as method C. The advantage is that the magnetic field cancelling effects are included with similar accuracy as method B. But inductances are represented as lumped elements which allows them to be more easily placed around the semiconductor die model inside the circuit simulator. The disadvantage is that the effective loop inductance is not as easily available as a single value for optimization tasks as in the case of method B.

The induced voltage across a lead of the package is dependent on both its own self-inductance and the mutual inductance it has to the neighboring leads. Thus for all of the three leads in Fig. 4 the equations are written in a compact matrix form as shown in (7). The result is a symmetric inductance matrix $\boldsymbol{L}$, where self-inductances are in the diagonal and mutual inductance terms are in the off-diagonal.

$$\begin{bmatrix} v_1 \\ v_2 \\ v_3 \end{bmatrix} = \frac{\mathrm{d}}{\mathrm{d}t} \begin{bmatrix} L_{11} & L_{12} & L_{13} \\ L_{21} & L_{22} & L_{23} \\ L_{31} & L_{32} & L_{33} \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \\ i_3 \end{bmatrix} \tag{7}$$

For a linear system, $L_{12} = L_{21}$, $L_{13} = L_{31}$ and $L_{23} = L_{32}$, thus the matrix is symmetrical. For smaller systems the mutual inductance couplings can be entered into the circuit simulator manually. However, for larger systems with a total of $N$ lumped elements, it is represented by a triangular $N \times N$ matrix, which includes $N$ self-inductances and $\frac{N(N-1)}{2}$ unique mutual inductances. This becomes impractical to enter manually in a circuit simulator. In practice ANSYS Q3D Extractor allows for the export of the inductance matrix in a SPICE `.cir`-format. Thus to use the result, it requires a SPICE compatible circuit simulator with some of the most common software being LTspice, Saber or Simplorer. Combining the electrical parasitics with the semiconductor die model provides assessment of device switching performance. It provides insights and enables the designer to identify and mitigate issues early in the design process, such as excessive ringing, voltage overshoots or parasitic turn-on. Ideally, this reduces the required amount of iterations of physical prototypes to be built.

## III. Thermal Impedance and Cross-Coupling Effects

A key aspect of the power module packaging is to ensure that the semiconductor devices are properly cooled. Thus early on in the design process the engineer must consider how much the semiconductors are heated due to the power being dissipated during operation. A simulation of the power loss is obtained using a detailed semiconductor model and including the electrical parasitics as discussed in the previous section, which provides a good approximation of switching and conduction loss. This is used as the input for the thermal model to predict the junction temperature. For most applications of power module packaging the general problem is to transfer the heat from a semiconductor through its various layers. Thus the problem is heat transfer in solids, which is given by

$$q = -k\nabla T \tag{8}$$

where $q$ is the heat flux, $k$ is the thermal conductivity of the solid material and $\nabla T$ the local temperature gradient. Compared with the highly coupled electromagnetic phenomena (1)-(6), heat transfer in solids (8) is relatively easy to solve.

One of the challenging aspects is to model the boundary condition for a baseplate or heatsink, especially in the case for liquid cooling. Solving the liquid cooling system involves dealing with a computational fluid dynamic problem which is significantly more difficult. From the perspective of the power module, the cooling performance is often evaluated on the

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bottom of the base plate by using a boundary condition of a convective heat transfer.

$$q = h\Delta T \tag{9}$$

where $h$ is the heat transfer coefficient, and $\Delta T$ is the temperature difference between the surface and the bulk fluid. The heat flux is then integrated for the whole surface to obtain the total power dissipated. Typically, $h$ is in the range of 100-300 $\frac{\mathrm{W}}{\mathrm{m^2K}}$ for forced convection of air, 500-2000 $\frac{\mathrm{W}}{\mathrm{m^2K}}$ for power modules in contact with a heatsink and 10000 $\frac{\mathrm{W}}{\mathrm{m^2K}}$ or more for liquid cooling [4], [14], [54]–[56].

Instead, one of the main considerations is how to utilize the calculated temperature distribution after a thermal FEA, and combine it efficiently with the semiconductor model and the lumped electrical parasitics. Solving the full 3D structure of a power module is time consuming, and thus solving the thermal distribution in the entire structure for each time step together with the electrical model from Section II results in impractical long simulation times. The general approach is to transform the thermal domain into lumped RC-elements, to model the thermal resistances and thermal capacitances. The RC elements are arranged in typically two different representations being Cauer and Foster networks. For the Cauer network, as shown in Fig. 5(a) the values of the RC-elements can be extracted from physical quantities. For a block of cross sectional area $A$, and thickness, $d$, the thermal resistance is

$$R = \frac{d}{k \cdot A} \tag{10}$$

where $k$ is the thermal conductivity of the material. The heat capacity can then be calculated as

$$C = c \cdot d \cdot A \tag{11}$$

where $c$ is the heat capacity of the material. Alternatively, it is demonstrated that the values of the RC-elements can be extracted node by node from the thermal response simulated in a FEM software [57]. An advantage of the Cauer network is that the RC elements have physical meaning, by which a Cauer network of a semiconductor obtained from the datasheet can be connected with a Cauer network of a PCB, power module, heat sink etc. Thus, because the Cauer network represents physical thermal resistances and capacitances, the temperature in the interface layer i.e. temperatures at solder layers are observable with the Cauer model. To include cross-couplings, the Cauer network is expanded into a 3D structure [58]–[60], as shown in Fig. 5(b). Such a model can be regarded as a coarsely meshed finite element representation. In many cases, the main purpose is to obtain the junction temperature used as the input for the semiconductor model, and thus calculating the temperature in other nodes is wasting computing power. This is one of the reasons Foster networks are often used, as they only represent the large-signal behavior.

A Foster network is shown in Fig. 6(a). In contrast to the Cauer network, the internal nodes of the Foster network do not have physical meaning. Analyzing Fig. 6(a) using Kirchoffs current law, all the thermal power flowing into the circuit must also exit the network, meaning that all the individual RC lumps see the same thermal power simultaneously. Thus the

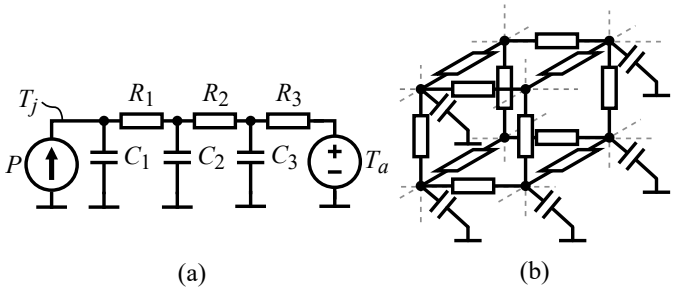


Fig. 5: Lumped RC-elements arranged as (a) 1D and (b) 3D Cauer-networks.

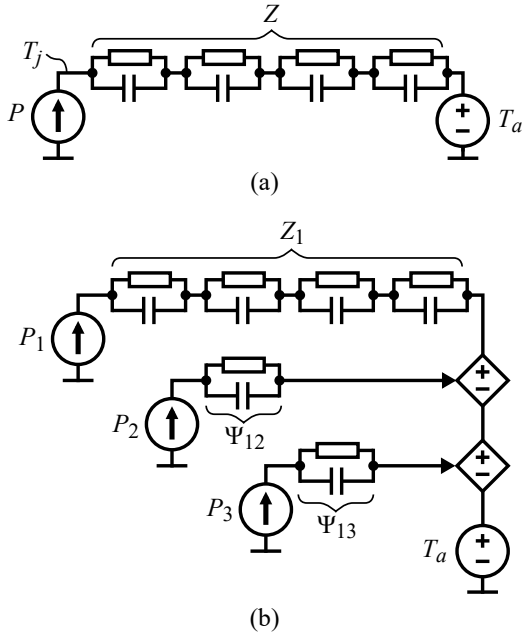


Fig. 6: Lumped RC-elements arranged as (a) single and (b) coupled Foster-network.

Foster network uses super-position of different time constants to model the same signal-behavior as the original 3D geometry. Due to the super-position, the location of the different RC-elements are interchangeable. The thermal impedance, $Z_i$, of a device $i$ in the power module is defined as

$$Z_i(t) = \frac{T_i(t) - T_a}{P_i(t)} \tag{12}$$

where $T_i$ is the temperature of device $i$, $T_a$ is the ambient temperature and $P_i$ is the power dissipation in device $i$. Having obtained a time-dependent thermal impedance, the different RC time constants are extracted from curve-fitting. Often the thermal behavior is represented by only 3 to 5 RC-elements and still obtain good accuracy, and thereby it is computationally efficient.

In addition to the thermal impedance of the semiconductor device itself, it is often desired to include the thermal coupling that the device has to the neighboring devices. For this, a thermal coupling parameter, $\Psi$, is defined as

$$\Psi_{ij}(t) = \frac{T_i(t) - T_a}{P_j(t)} \tag{13}$$

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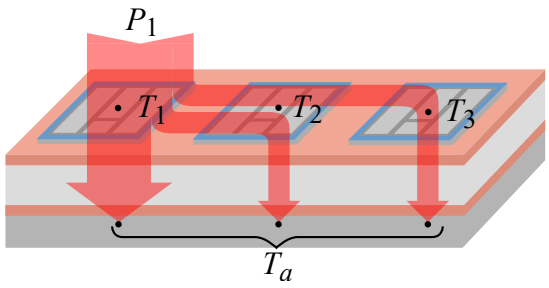


Fig. 7: All power dissipated in a device flows to the ambient $T_a$, but some of the power heats up neighboring devices along its way.

where $T_i$ is the temperature of device $i$ and $P_j$ is the power dissipation in a neighboring device $j$. Thus $\Psi_{ij}$ is read as the temperature increase of device $i$ caused by the power dissipation of device $j$. While the definition of thermal impedance in (12) and the coupling parameter (13) look similar, it is important to note the difference. For the thermal impedance, $Z$, it is required to know the path of the power flow. This is valid for the self-heating of a device, as power loss is at the junction of the device and eventually must end up at the ambient environment, as shown in Fig. 7. In a practical case, the amount of power which flows between the different devices is difficult to measure, and thus cannot be regarded as a thermal impedance. Instead, the coupling parameter, $\Psi$, is introduced to model the temperature increase as a function of the power loss in a neighboring device, as this quantity is directly obtained from a SPICE simulation.

For the case of a power module with a total of three semiconductor devices, (12) and (13) are applied to all devices and combined in a compact matrix form [61], [62] given by

$$\begin{bmatrix} T_1 \\ T_2 \\ T_3 \end{bmatrix} = \begin{bmatrix} Z_1 & \Psi_{12} & \Psi_{13} \\ \Psi_{21} & Z_2 & \Psi_{23} \\ \Psi_{31} & \Psi_{32} & Z_3 \end{bmatrix} \cdot \begin{bmatrix} P_1 \\ P_2 \\ P_3 \end{bmatrix} + T_a \qquad (14)$$

The coupled Foster network for one of the devices can then be implemented as shown in Fig. 6(b). In summary, the thermal characteristics of the semiconductor devices in a power module are typically extracted using the following steps:

1) Apply a step power input to device $i$ of the power module.
2) Monitor temperature of device $i$ and apply (12) to obtain the thermal impedance.
3) Monitor temperatures of neighboring devices and apply (13) to obtain their thermal couplings.
4) Redo step 1-3 for all individual devices in the power module.
5) Use curve-fitting to find the first-order time constants of the system and evaluate the equivalent RC-lumped network parts.

The Foster network is advantageous from a practical point of view because the same procedure is used for both the experiment and the simulation. This makes it easy to compare the two as the raw data is treated similarly. By introducing the thermal coupling, $\Psi$, for building up the Foster network, it is not necessary to know the exact path of the power flow, which otherwise is a hard quantity to obtain in the case of an experiment. Compared with the 3D Cauer network, the coupled Foster structure is relatively computationally efficient. Also, the number of lumped RC-elements is easily decreased depending on the desired accuracy. However, for a large number of interconnected dies even the coupled Foster network becomes computationally heavy, and alternative implementations are proposed to reduce the simulation time [63], [64].

### *A. Case study: Simulation of thermal impedance in an integrated PCB/DBC power module*

New integrated packaging solutions are being proposed to utilize the faster switching speeds offered by new WBG devices. Recently both the DBC and PCB is being combined into single switching cell packages, with parasitic inductances in the range of 1-3 nH. However, for the literature presenting the thermal analysis of these packages, the simulation is done without modelling the PCB [14], [16], [65]. This section presents a case study of the extraction of the thermal characteristics of an integrated GaN eHEMT power module which includes the PCB in the analysis [66].

The power module uses 650 V GaN eHEMT devices from GaN Systems [67]. The devices have a solderable heat pad on the bottom which is soldered to a DBC, as shown in Fig. 8. The top side of the device has electrical connections for gate, drain and source, soldered to a PCB which has DC-link capacitors, gate drivers and measurement circuitry. Thus the GaN eHEMT device is sandwiched between a DBC and PCB, which ensures a structure with both low inductance and low thermal resistance. The assembly is designed in Solidworks and imported to COMSOL Multiphysics for the FEA. More details on the software methodology is presented later in Section V. The goal is to investigate the thermal characteristics of this entire assembly with and without the influence of the PCB.

A power step is given to the device labelled as “1”, and the transient thermal response of all four devices is monitored. The thermal impedance of the device under self-heating is calculated using (12), while the thermal coupling to neighboring devices is calculated using (13). The results are shown in the solid lines of Fig. 9. After this an insulation barrier is inserted at the top-side electrical contacts of the GaN eHEMT devices, meaning that none of the injected power is transmitted through the layers of the PCB. A simulation is run once more and the obtained results are shown as the dashed lines in Fig. 9. The results show that thermal impedance of the device under self-heating experiences an increase of 13 %. The thermal resistance laterally through the thin copper layers is relatively high, but the thermal paths of the three neighboring devices are in parallel with the main path, which is dominantly through the DBC area under the device itself. Thus, in conclusion failure to correctly include the influence of the PCB in an integrated power module can result in significant error in the prediction of the thermal performance [66].

### *B. Thermo-mechanical induced stress*

Once the thermal distribution has been simulated, it allows the designer to assess the result and make necessary changes.

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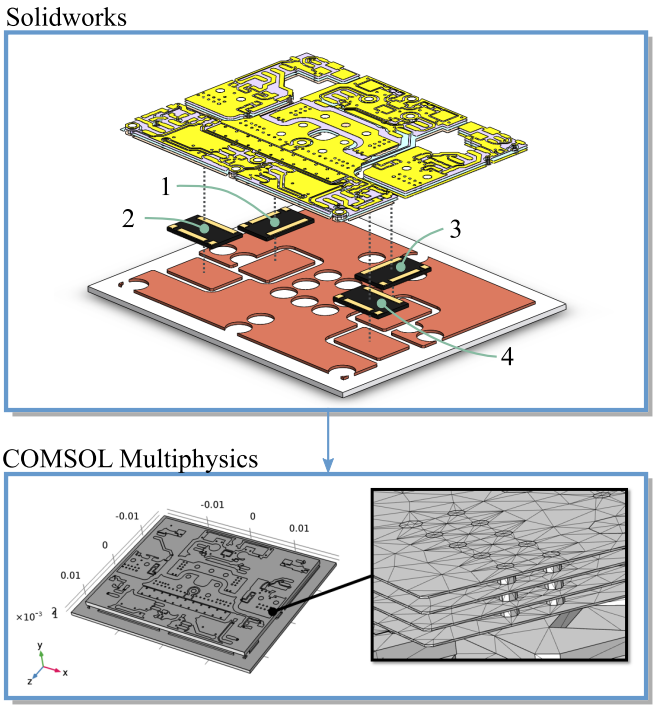


Fig. 8: A 3D model of an integrated GaN eHEMT power module is imported to COMSOL to simulate the thermal characteristics.

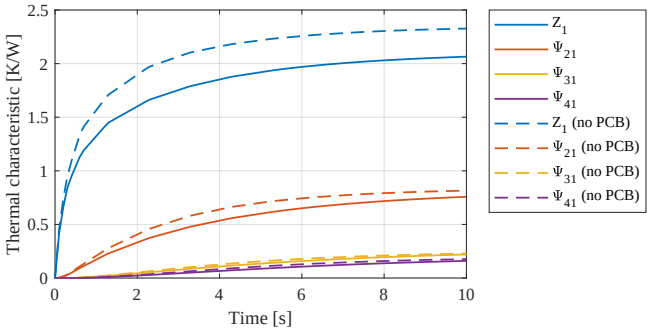


Fig. 9: Thermal response of the four devices in the studied package, with and without the influence of the PCB.

As an example, a PCB board experiences localized hot spots due to current crowding. In literature, multi-physics FEM is used to investigate how the copper thickness and placement of vias is crucial to avoid hotspots in high power PCBs [68]–[70]. Following the thermal simulation, it is possible to add mechanical parameters to the materials and solve for the thermo-mechanical induced stress. Commonly, failure modes in power electronics are related to the differences in coefficient of thermal expansion of materials. Together with parameters of Young's modulus and Poissons ratio a simulation of the stress/strain inside the materials are mapped.

The FEA solutions highlight localized issues where high mechanical stresses occur, which allows for the designers to take action [71]. This can be used to mitigate problems that can cause failures early. If materials are stressed outside their elasticity region, it means that permanent plastic deformation occurs and can be identified as an imminent source of reliability issues. Simulating the life-time of a material which is stressed only within its theoretical elasticity region is more difficult. Commonly, the predictions are relying on experimental life-time data obtained through power cycling at accelerated stressor levels [72]–[74]. The reason being, that materials change over time, due to phenomena such as metallization degradation [75], mass diffusion due to current cycling [76] or propagation of cracks [77]. Phenomena such as these cause difficulty to predict the life-time solely by using FEM, as the phenomena are not significantly present initially in the product life-time, and because they occur on a micron-scale compared with the full package size. Instead a component library is established based on experimental wear-out tests. FEA is used to create accurate electro-thermal reduced order models, utilized to simulate accumulated damage over time to predict the life-time under different scenarios [78]. A disadvantage is that the experimental data of wear-out is linked to a specific component, meaning that it is not directly transferable to new designs. A shift from component life-time libraries, to a physics-of-failure approach (i.e. accumulated damage is calculated per failure-mode, not on a component-level), is mentioned as a possible solution to better predict life-time early in the design phase [79], [80]. However, at the time of writing such approaches are not widely used within the field of power module packaging, and experimental component wear-out tests are still the most commonly used approach.

## IV. Electric fields

Evaluation of electric fields strengths is an important step in the verification of a power module layout to ensure safe operation. The ability to withstand high electric fields is one of the key benefits of using DBC and power modules. Design of power modules to withstand high electric field strengths is inherently linked to high voltage power modules, with renewed interest due to the recent availability of 10 and 15 kV SiC MOSFET devices [42]. The electric fields in conventional power module structures have been studied in detail, with several proposals to reduce peak electric fields by: choosing an encapsulant with advantageous permittivity [81], coating of the ceramic edge [82], stacking of ceramic substrates [83] or incorporating grooves in the ceramic [84]. However, design of the power module layout to distribute electric fields is also important for low voltage power modules. To increase the power capability, the thermal resistance should be as low as possible, meaning that insulating layers of typically ceramics or FR4 are made thin. Even a low voltage applied to a thin layer may produce higher electric field strengths compared with power modules operated at several kilovolts [4], [5]. In conclusion, maintaining a safe operating margin of the electric field strength and keeping a low thermal resistance is often a compromise, and thus understanding of both problems is important to achieve a good performing power module.

### A. Mesh dependency

An issue when evaluating the electric field is that it is heavily dependent on the mesh of the finite element simulation. To

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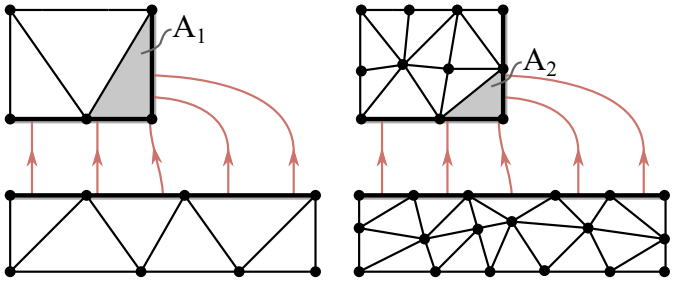


Fig. 10: Reducing the mesh size might locally increase the calculated electric field strength due to field crowding.

understand this it is compared with the two previous problems related to the evaluation of inductances and heat transfer. For the inductance, the magnetic field is integrated over the enclosing surface. Thus discrepancies in the mesh that results in a localized spike in the calculated field intensity are mitigated as the field is integrated. Similarly, for the heat transfer in solids the heat flux is integrated over the surface to obtain the full power dissipated, and as such can be considered a macroscopic quantity. However, when evaluating the electric field the concern is on the localized effects and to observe the regions at which the electric field is strongest. In the final power module it is these regions where an electric field breakdown or substantial partial discharge may occur.

In general for FEA it is expected that using a finer mesh results in higher accuracy of the obtained results, but this is not always the case when evaluating the electric fields. Field crowding occurs around the edges and corners of the high voltage energized copper traces of the DBC. Calculating the field in these regions has a strong mesh dependency as reported in literature [85], [86]. The issue is explained using the finite volume representation shown in Fig. 10. Defining the electric field strength as the number of field lines entering a cell, divided by the circumference of that cell. The number of electric field lines entering $A_1$ and $A_2$ is the same in the two cases. As the circumference of cell $A_2$ is smaller than $A_1$ the evaluated electric field strength of $A_2$ is higher. In fact, for finer and finer meshes the calculated electric field strength approaches infinity.

The mesh dependency can be reduced in some models if the field is uniformly distributed in some regions by integrating along an edge or surface. For instance by adding an additional dimension to Fig. 10 perpendicular to the 2D surface shown and averaging the result over several cells. In [87], [88] an edge radius is used to reduce the mesh dependency. The hypothesis is to obtain a convergence point for the electric field strength, compared to the case of a sharp rectangular corner. Although a convergence point is obtained, the convergence point then depends on the chosen edge radius. In [86] several measurement points at a small distance and angle from the edge corner are used. Using this approach the field is evaluated away from the point which causes the singularity. A parametric sweep of the distance and angle of the measurement points around the edge show that a mesh-independent calculation of the electric field strength is possible. A mesh-independent approach is important to numerically evaluate the maximum

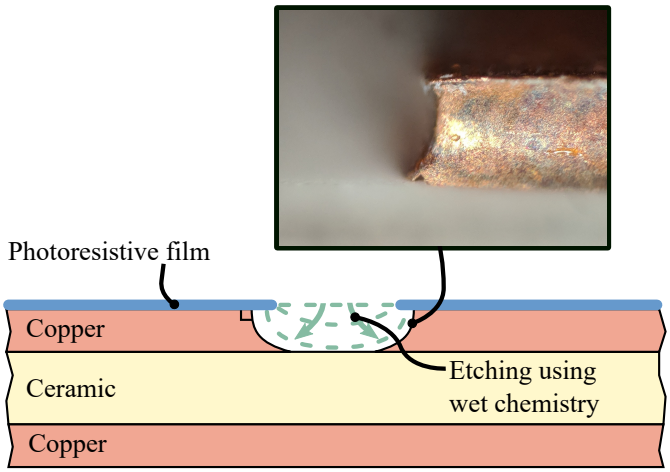


Fig. 11: Wet chemistry used for etching produces a snowplow-shape of the copper edge.

electric field strength to compare different designs of the power module layouts.

### B. Model discrepancies

Because of the nature of the problem when studying the localized electric field densities, there is also stronger influence of discrepancies in the model, when compared to the problem of extracting inductance or thermal impedances. Here we define discrepancies in the model as small mismatches between the physical world and our digital 3D model of the geometry, such as groins on a busbar, voids in an interface or curvature of the copper trench. Again, a few voids in a layer might only slightly alter the heat transfer. However, for electric fields a void could be the local initiation point for partial discharges. Continuous energy discharges in a region potentially deteriorates its properties over time, which eventually leads to an electric field breakdown [4]. The breakdown strength of dielectric materials is known to change over time related to factors such as temperature and humidity [81], [89], and thus such considerations must be taken into account and proper design margins should be chosen.

In most of the simulation models of electric fields in a power module, the 2D crosscut of copper traces are regarded as rectangular shapes [81], [83], [86], [88], [90], similar to what was shown in Fig. 10. In real applications a photo resistive film is applied to the copper, and a wet chemistry process is used for etching of copper traces, as shown in Fig. 11. Due to this etching process, copper is removed not only downwards toward the ceramic, but also laterally which causes a “snow plow”-shape. As reported the high electric field density may initiate partial discharges at the interface between the triple point and the air/encapsulant around the sharp edge inside the trench [91]. In [88] the influence of a 5 $\mu$m thin protrusion of the copper trace at the edge of the ceramic is reported to increase the electric field density by a factor of 2.

Due to the degradation of material properties and model discrepancies in the simulation model, experimental testing of a manufactured prototype in terms of a partial discharge

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test is still widely used [4], [85], [91]. While experimental verifications are important, the widespread use within the topic of electric fields can also be a sign that there is currently not a full trust in the simulated results. Compared with the literature of electrical parasitics and thermal analysis, in Section II and III respectively, the simulation is regularly used as the main source for analysis. At the time of writing, electric field simulations are regarded a useful tool to digitally iterate layouts that limits the electric field intensities. However, in terms of verifying layouts purely digitally there is still research to be performed to reduce uncertainties, when compared to the fidelity at which simulation of electrical parasitics and heat transfer are currently used.

## V. Digital design framework

The purpose of digital design is to reduce development time by limiting the number of physical prototypes to be built. Within electronics there is typically a relatively short lead time of components and PCBs. This makes it tempting to quickly move to an experimental testing phase to try out a design. This is a trial and error approach. However, if designs are iterated several times, the lead times may start to add up. Additionally, if a complex problem is encountered, it may be difficult to identify, measure and validate a possible solution. A good digital design framework should allow the engineer to digitally iterate through several designs on a daily basis. Furthermore, it should give additional insights in internal states/quantities of the electronics system to help identify and solve challenges in the design. If used correctly, it is only required to build a single physical prototype fulfilling the design specifications. This section presents an example of a general digital design framework, followed by a practical example of the design of an integrated GaN eHEMT switching cell.

An example of a digital design framework is proposed in Fig. 12, which combines and summarizes the topics covered through Section II to IV. Such a framework employs different simulation software packages, which are developed with a focus on solving a specific type of problem. This is advantageous because the simulation is split into smaller sub-problems, which reduces the computational complexity and thereby reduces convergence issues. The alternative is to use a single multi-physics environment to treat all problems simultaneously. While this allows for a fully coupled solution, it causes difficulty within the topic of power electronics, because of the difference in time constants between high frequency electromagnetics, slow thermal transients and static electric fields. Most modern software packages are designed for efficient multi-core processing. By splitting the problem into several smaller sub-problems in different software packages, it even allows the simulations to be run in parallel on more computers at once. However, when the problems are split into several software it must be ensured that the file import/export capabilities of each software is compatible with one another. A practical case study of the software interactions, used to design an integrated GaN eHEMT switching cell, is presented in the following section.

### *A. Case study: Design of integrated GaN eHEMT switching cell*

The digital design framework of Fig. 12 displays a general approach. In practice, it is important to make sure that the different sub-tools used, are capable of exchanging information from one software to the other. The following demonstrates a real design case of an integrated GaN eHEMT full-bridge switching cell, that was already briefly introduced in Section III-A.

The software utilized to build up a 3D model and to analyze the integrated switching cell structure is summarized in Fig. 13. The PCB structure was designed using the layout software PADS. The PCB layout editors work with 2D information on different layers, and thus does not explicitly contain a 3D description of the PCB. The PCB software allows for the export of a 3D model, but this is typically a mechanical outline and does not include all trace information on the inner layers. To build a 3D model of the PCB, the 2D layer information is imported into ANSYS Electronics Desktop. This software reads the 2D layer information and creates a 3D model including copper layers, vias and pads of components. The 3D model is imported to ANSYS Q3D Extractor. The lumped parasitic elements are modelled by Method C as described in Section II-A. This model is exported to LTSpice which also uses the device models supplied by the semiconductor manufacturer. The simulation and experimental results are compared in Fig. 14, for a double pulse test performed at 400 V and 15 A. The results show the ability to simulate switching speeds even in the range of 5 ns and voltage transients of 64 V/ns [16].

Following this step, the 3D model of the PCB is imported into Solidworks and assembled with the other 3D models of the GaN eHEMT devices and the DBC. The Solidworks-assembly also validates that all parts mechanically fit together and provides insights on tolerances for manufacturing. The assembled 3D model of the integrated switching cell is imported into COMSOL Multiphysics. The model requires a relatively fine mesh to include the details around the vias and the thin copper layers of the PCB. A workstation with 64 GB of memory is used for the simulation. This is the same simulation model as was presented in Section III-A. The simulation model was validated by experimentally measuring the device temperatures. The device temperatures are monitored using fiber optic temperature sensors, and resulting thermal characteristics are shown in Fig. 15 [66]. The thermal response is modelled by RC-elements using the Foster-network and implemented in LTspice to create a thermo-electrical circuit model. The solved temperature distribution is also used in COMSOL Multiphysics as the input for a thermo-mechanical simulation. Due to the temperature distribution and mismatch in coefficients of thermal expansion of materials, the switching cell experiences a mechanical stress and strain. The purpose of the simulation is to map the locations of highest mechanical stress. Future research is focused on validation of this thermo-mechanical model, and to perform temperature cycling of the real module to verify if the simulation is capable of predicting the locations of failure.

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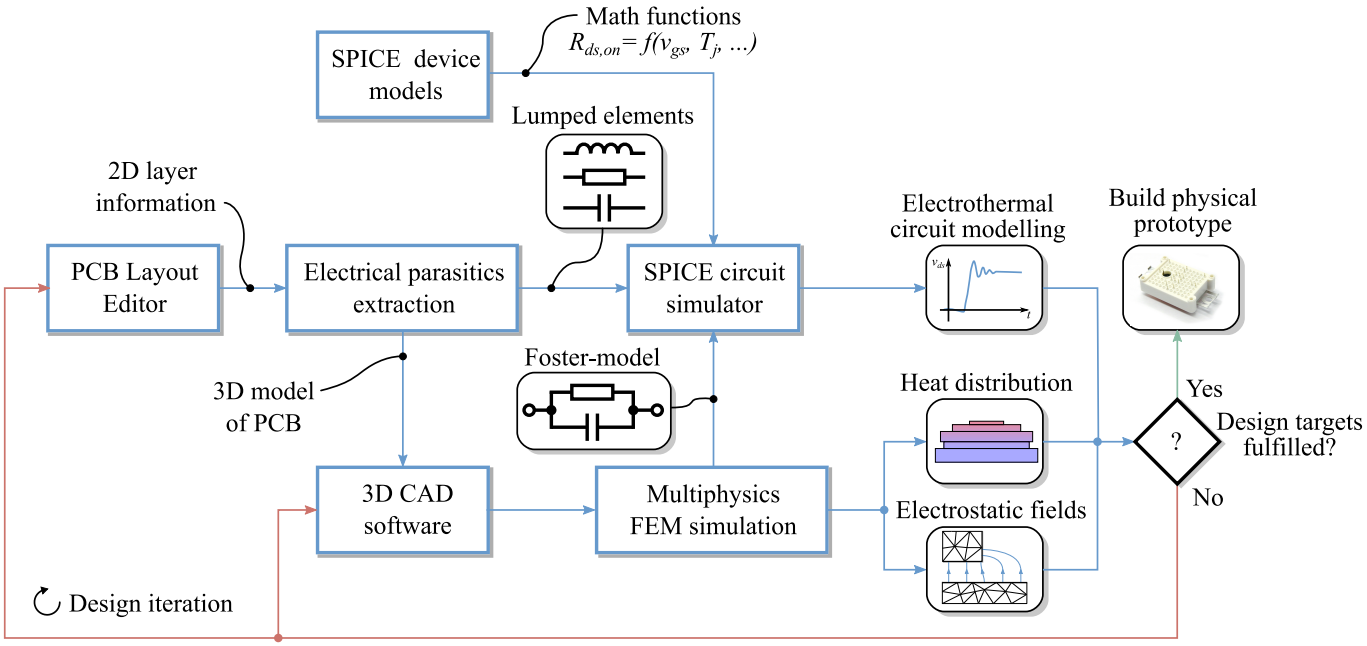


Fig. 12: An example of a general framework used for digital design of power modules.

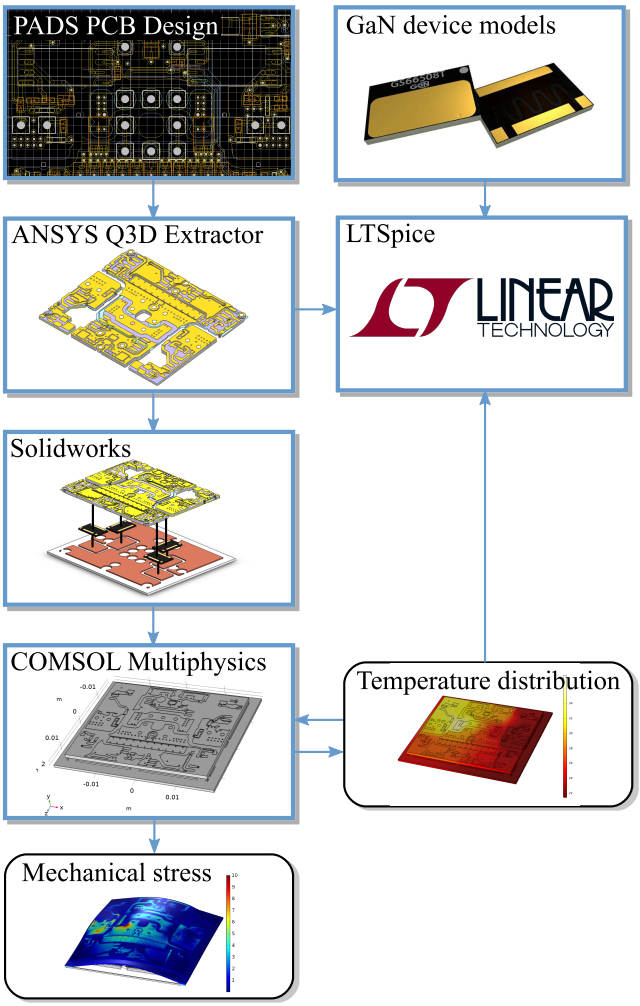


Fig. 13: Software framework used for digital design of an integrated GaN eHEMT switching cell.

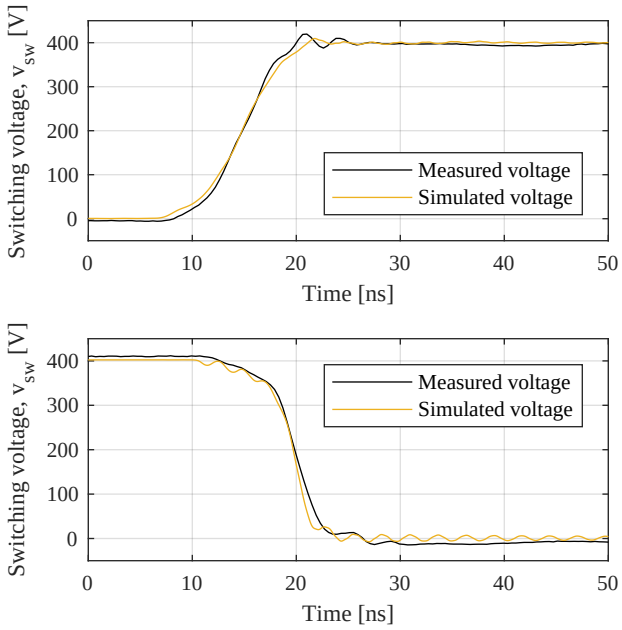


Fig. 14: Simulated and measured voltage waveforms during turn-on and turn-off at 400 V / 15 A.

## VI. Discussion and Future Challenges

As the topic of using digital design is growing in power electronics design, it is relevant to discuss the future aspects in this regard. Combined with the increasing switching speeds owing to the superior characteristics of WBG semiconductor devices compared with Si, it is important to cover some of the potential future challenges linked to the use of FEA.

The currently popular electrical parasitics evaluation software based on the quasi-static assumption i.e. FastHenry2, ANSYS Q3D Extractor are likely to face issues as the switching

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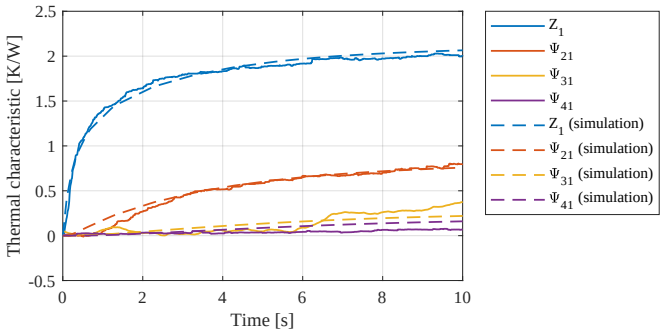


Fig. 15: Simulated and measured thermal impedance and thermal cross coupling of each device.

speed is continuously increasing. Eventually full-wave solvers are required for accurate modelling, as the interaction between transient electric and magnetic fields become more significant. The gap between power electronics engineering and circuit design at radio frequencies (RF) will narrow, and the experiences gained from the RF industry are to some extent expected to be merged into the power electronics discipline [92]. At RF the higher order transmission line networks or S-parameters are often employed, in comparison with the computationally efficient reduced order model RLC lumped elements often used in power electronics. In [93] parasitics of a GaN device are extracted using S-parameters, as this approach is more suited with inductances and capacitances in the order of less than 1 nH and 1 pF, respectively.

This overview has described the combination of semiconductor die behavior with PCB parasitics, i.e. mainly the components associated with the power loop. To fully unlock the potential of digital design, more and more components are to be included in the framework. A next step is to predict behavior of main components in the gate-driver and control circuitry such as: gate drivers, linear voltage regulators, Schmitt triggers or buffer-circuits. Including these components in the simulation framework enables evaluation of system performance as high frequency differential and common mode noise propagates through the circuitry due to the fast switching speed of the WBG devices. Few manufacturers provide detailed models of IC behavior, i.e. how slew rates and propagation delays change on fluctuations on $v_{dd}$, $v_{ss}$ or signal inputs. For many components such information are still not readily available, which then leaves a gap in the digital design process. In [94] a frequency-dependent model is extracted of an IC from the more simple I/O buffer information specification (IBIS) provided by most manufacturers. IBIS representation describes IC behavior without revealing internal workings, and typically work as a transfer function to include delay and slew rates on the output based on input. However, fast evaluation of several designs, depend on access to detailed and readily available semiconductor die and IC models.

Despite these challenges and current shortcomings, the potential reduction in development time as well as long term benefits cannot be understated [95]. Industry 4.0 suggests expansion of digitalization throughout the full product life-cycle which depend on available 3D geometries of each part. However, for usefulness of the developed models it is just as important to reduce the computational efforts to match the use case. Computationally efficient models of the system are prerequisites in the development of digital twins. These are digital replicas emulating the current state and performance of a product in the field. Harvesting data from the field and using this in real-time to predict and monitor the operation of a power module or converter, requires accurate but computationally efficient simulation models [96]. In conclusion, unlocking the potential offered by Industry 4.0 begins with the use of digital design.

## VII. Conclusion

This paper presents an overview of simulation tools and methods used in the digital design of power module packaging. Three main benefits of power module packaging are reduction of electrical parasitics, improved thermal management and operation at elevated voltage levels. These three topics are the main aspects treated in regards to digital design. A discussion of solvers for Maxwells equations is given in regards to extraction of electrical parasitics, and ANSYS Q3D Extractor is highlighted as a popular extraction tool within the topic of power module packaging. The literature review describes different approaches in the use of ANSYS Q3D Extractor, which are classified into three methods and a discussion of advantages/disadvantages is presented for each. For the thermal management, implementation of the simulated temperature distribution is a main consideration, with the Cauer and Foster networks being the two dominant representations. Cauer networks resemble the physical quantities, and in that sense are regarded as a coarsely meshed finite element representation. For multichip modules the coupled Foster network is typically more computationally efficient, while maintaining good accuracy and easy implementation in a common SPICE simulation environment. A case study presents an integrated power module based on GaN eHEMT devices, combining DBC and PCB in a single switching cell. The results show an error of 13 % in the simulated thermal impedance if the PCB board is not included in the model. For simulation of electrical field densities, mesh dependency and model discrepancies are highlighted as two main challenges. Because of this, the experimental testing of partial discharges is still widely used, and thus is currently a challenge in terms of utilizing digital design to its full potential. As the mesh is decreased in size and due to electric fields crowding at sharp edges, it results in simulated peak electric field densities approaching infinity. Averaging over several nodes or defining measurement points slightly away from the points causing the singularity are the common solutions. Model discrepancies such as voids or sharp edges seen in real applications cause localized electric field densities, which are generally not covered by the simulation. At last a simulation framework is proposed which allows to study the beforementioned problems even with compact integrated power module packages utilizing both PCB and DBC. Future challenges are discussed such as the increase in necessary solution frequencies and inclusion of more detailed IC component behavior. Digital design and FEA is concluded

as a prerequisite for several aspects covered by Industry 4.0, and thus the use of digital design tools is only expected to increase in years to come.

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**Asger Bjørn Jørgensen** received the M.Sc. Energy Engineering with a specialization in Power Electronics in 2016 and the Ph.D. degree in 2019 from Aalborg University, Denmark.

He is currently working as a Postdoc at the Department of Energy Technology, Aalborg University. His research interests include power module packaging, wide bandgap power semiconductors and multi-physics finite element analysis.

**Stig Munk-Nielsen** received the M.Sc. and Ph.D. degrees in electrical engineering from Aalborg University, Aalborg, Denmark, in 1991 and 1997, respectively.

He is currently working as a Professor WSR at the Department of Energy Technology, Aalborg University. He has been involved or has managed 12 research projects, including both national and European Commission projects. His research interests include low and medium voltage converters, packaging of power electronic devices, wide bandgap semiconductors, electrical monitoring apparatus for devices, failure modes, and device test systems.

**Christian Uhrenfeldt** received his M.Sc. in Physics from Aalborg University in 2004. In 2008 he received the Ph.D. degree in the field of semiconductor material science from Aarhus University.

He is currently working as Associate professor at the Department of Energy Technology at Aalborg University on power electronics packaging and materials. His research interests include packaging of power modules, nondestructive testing and semiconductor diagnostics in power electronics.